Ultra-Low Loss Build-up Film for Fine Pitch Applications, "AS-500HS"

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1 Abstract

With the recent expansion of globalization and cloud services, devices used for server and wireless communications need to transmit large amounts of data at high speed. Thus the semiconductor components of such devices must be able to handle high-speed and wide-band signal transfers. To satisfy these requirements, we have developed a new ultra-low loss, build-up film (AS-500HS).

"AS-500HS" is processable for semi-additive processes, shows only small surface roughness after chemical roughening (Ra:220nm), and has a high peel strength with plated copper (0.7kN/m). Moreover AS-500HS shows a low dissipation factor (0.0034), low CTE, high heat resistance, and excellent reliability.

2 Characteristics of the Product

- It has an excellent dielectric dissipation factor (0.0034) and a low coefficient of thermal expansion (17 ppm/°C).
- It allows fine-pitch wiring formation with a line and space (L/S) ratio of 2/2 μm.
- It provides high insulation reliability to L/S=2/2 μm fine-pitch pattern circuit (no insulation deterioration for 200 hours or more under test conditions of 130°C/85% RH and applied voltage of 3.3 V).

3 Background of the Development

Following the full-scale opening of the IoT Age, needs are mounting for high-speed, large-capacity data exchange.[1)] Accordingly, the mainstream method of fabricating semiconductor mounting substrates (semiconductor packages) is now the semi-additive process (SAP), which allows wiring pitch reduction, density enhancement, and thickness reduction.[2)] Wiring pitch reduction, however, causes an increased transmission loss, which can easily lead to signal quality deterioration. It is known that the transmission loss is proportional to the dielectric constant (Dk) or the dielectric dissipation factor (Df), and the roughness (Ra).[3)] Therefore, it is important to reduce Dk, Df and Ra. Moreover, semiconductor package thickness reduction leads to a lower rigidity of the chip mounting substrate. Hence, it is also important to reduce the warpage caused by the difference in the coefficient of thermal expansion (CTE) between the chip and the substrate. Accordingly, there is a need for a SAP-compatible, build-up film that features excellent dielectric properties (Dk ≤ 3.3 and Df ≤ 0.0040), a low CTE (20 ppm/°C or less), and a small Ra (250 nm or less).[4)]

Then, we embarked on the development of a build-up film incorporating our proprietary primer resin technology, low dielectric resin technology, and low CTE resin technology.

4 Technical Details

1. Development Concept of "AS-500HS"

In SAP, build-up film first undergoes chemical roughening by desmear and then electroless copper plating. Therefore, the adhesion to the electroless copper plating layer is critically important from the perspective of stable multilayer substrate manufacturing. On the other hand, the resin approach to transmission loss reduction or CTE reduction requires the use of a low-polarity material or an increased amount of filler and hence is disadvantageous to achieve high adhesion strength. Accordingly, we applied, to "AS-500HS", a bifunctional structure (bilayer film structure) that consisted of a primer layer having a low-roughness roughened surface morphology and high adhesion properties advantageous for fine-pitch wiring formation, and a base resin layer for developing low dielectric properties and a low CTE.

2. General Properties of "AS-500HS"

Table 1 shows the general properties of "AS-500HS", which shows good dielectric properties including a Dk of 3.3 and a Df of 0.0034 at 5 GHz. Its CTE is reduced by approximately 60% (17 ppm/°C) compared with our existing proprietary product.[4] Moreover, when it has small surface roughness after desmear treatment (Ra: 220 nm), it exhibits strong adhesion to the copper plating layer (0.7 kN/m). This characteristic is advantageous for fine-pitch wiring formation and enables line formation with an L/S of 2/2 μm (**Figure 1**). At the same time, this wiring region shows high insulation reliability. Furthermore, the via bottom resin residue left after laser via formation is completely removed by desmear, thereby providing SAP processability.

3. Transmission Characteristics of "AS-500HS"

Figure 2 shows the evaluation results of the transmission characteristics (transmission loss) of "AS-500HS" micro-strip line. "AS-500HS" has lower transmission characteristics, in each temperature range, than our existing build-up films.[5]

Table 1 Properties of "AS-500HS"

Item		Unit	***AS-500HS***	AS-11G*3
Dk(5 GHz) *1	—	—	3.3	3.4*3
Df(5 GHz) *1	—	—	0.0034	0.0140*3
CTE	TMA(30-120℃)	ppm/℃	17	45*3
	TMA(250-300℃)		44	—
Tg	DMA	℃	233	165*3
Elastic Modulus	DMA(30℃)	GPa	12	2.4-2.6*3
Roughness*2	Ra	nm	220	300-400*3
Resin residue after desmear at via bottom*2	—	—	No residue	—
Peel strength*2	Cu plating	kN/m	0.7	0.7*3
Reflow cycle Resistance*2	260℃ reflow	cycle	20	—
Reliability at fine line space (L/S=2/2 μm) *2	130℃ / 85%RH, 3.3 V DC	h	200	—

＊1) Cavity resonator perturbation method
＊2) Treatment condition : Swelling 60℃ 10 min, Etching 80℃ 15 min
＊3) Catalog value

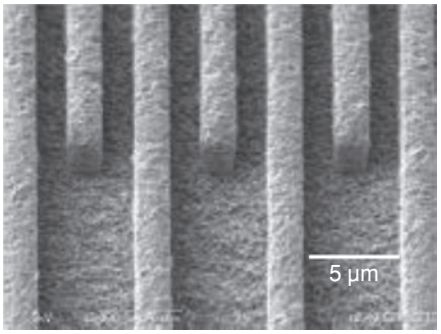

Figure 1 SEM image of L/S=2/2 μm on "AS-500HS" by SAP

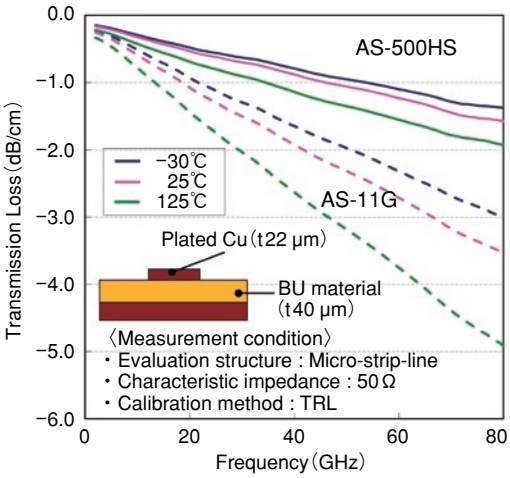

Figure 2 Transmission loss of "AS-500HS"

5 Future Business Development

・Development of build-up film with a further lower transmission loss and lower coefficient of thermal expansion.

[References]

1) International Technology Roadmap for Semiconductors, 2011 ed., SLA
2) Kiyoshi Takagi, Everything from Start to Finish on the Making of Build-Up Multi-Layer Printed Circuit Boards (2006)
3) Y. Mizuno,"Low Transmission Loss Multilayer PWB Materials for High-Speed and High-Frequency Applications", ECTC, 2013.
4) Shin Takanezawa, "Development of Ultra-Low CTE Substrate Material for Semiconductor Packaging," Journal of the Japan Institute of Electronics Packaging Vol. 19, No. 6, pp. 421-426 (2016)
5) Shin Takanezawa, "Build-Up Material AS-11G for Next Generation Packaging Substrates," Hitachi Chemical Technical Report No. 41 (2003))